Utku Aydonat

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Interests Compilers, static and run-time optimizations, parallel and distributed systems, microprocessor architecture, thread speculation, transactional memory, scalable synchronization.

Education

- **Doctor of Philosophy in Computer Engineering**, University of Toronto, 2011.
- **Master of Applied Science in Computer Engineering**, University of Toronto, 2005.
- **Bachelor of Science in Electrical and Electronics Engineering**, Middle East Technical University, Turkey, 2002.
  Major: Computer Engineering, *GPA*: 3.69 (out of 4.00).

Skills C, C++, Java, Perl, Linux/Unix operating systems, GCC/Open64/Suif compilers, parallel programming (pthreads, OpenMP, MPI), OS/161 systems simulator, Simplescalar processor simulator, Simics full system simulator, Gems memory modeling tool, Logic Design CAD tools, Verilog, assembly programming.

Work experience

- **Senior Design Engineer**, Altera Corporation Toronto Technology Center (May 2011 – Present).
  Responsibilities: Compiler support for the next generation Altera SOC architectures.
- **Research Assistantship – Ph.D. Thesis**, University of Toronto (January 2005 – November 2011).
  Thesis Title: Relaxing Concurrency Control in Transactional Memory.
  Area of Research: Improving the performance of Transactional Memory (TM) systems that ease writing high performance multi-threaded programs by reducing the need for thread synchronization.
  - Designed a novel algorithm that improves the concurrency of threads in TM systems by allowing conflicting transactions to commit successfully.
  - Implemented this algorithm in software as a C++ library and as well as in a hardware simulator that models the memory hierarchy of a CMP system.
  - Presented related publications at a major conference (MICRO) and at the principal venue of the research area (the TRANSACT Workshop).
- **Research Assistantship – M.A.Sc. Thesis**, University of Toronto (September 2002 – April 2005).
  Thesis Title: Compiler Support For A Multimedia System-on-Chip Architecture.
  Area of Research: Designing compiler transformations that parallelize multimedia applications for a novel System-on-Chip architecture.
  - Compiler transformations are based on static inter-procedural compiler analyses and extract task-level parallelism by analyzing and breaking the data dependences using privatization techniques.
  - Implemented the code transformations in a prototype compiler using the Open64 open source compiler.
  - Compiled and benchmarked real multimedia applications using this prototype compiler and demonstrated the scalability of the techniques.
  - Relevant papers were published in a major journal (IEEE MICRO) and received the Best Paper Award at the PDCS conference.

- ◇ **Teaching Assistantships**, Department of Electrical and Computer Engineering, University of Toronto (September 2002 – Present).
  Assisted Courses: Computer Architecture, Operating Systems, Programming Fundamentals, Computer Organization, Digital and Computer Systems.
  Responsibilities: Giving in-class tutorials, preparing assignment and exam questions, supervising laboratories, marking exams.
- ◇ **Internship**, Vestel Electronics, Turkey (Summer of 2001).
  Description: Contributed to the television picture stabilization project in the R&D department.
- ◇ **Internship**, Tubitak-Bilten, Turkey (Summer of 2000).
  Description: Studied VLSI digital circuit design and implemented an ALU unit.
- ◇ **Other M.A.Sc./Ph.D. Projects**:
  - · Implemented scalable locks in a distributed cluster.
  - · Implemented a memory leak detector for Windows binaries.
  - · Analyzed the .NET framework source code for run-time optimization opportunities.

PUBLICATIONS

U. Aydonat and T. S. Abdelrahman, *Hardware Support for Relaxed Concurrency Control in Transactional Memory*, IEEE/ACM International Symposium on Microarchitecture (MICRO), pp. 15-26, 2010.

U. Aydonat and T. S. Abdelrahman, *Hardware Support For Serializable Transactions: A Study of Feasibility and Performance*, Workshop on Transactional Computing (TRANSACT), 2009.

U. Aydonat and T. S. Abdelrahman, *Serializability of Transactions in Software Transactional Memory*, Workshop on Transactional Computing (TRANSACT), 2008.

T. S. Abdelrahman, A. Abdelkhalek, U. Aydonat, D. Capalija, D. Han, I. Matosevic, K. Stewart, F. Karim, A. Mellan, *The MLCA: A Solution Paradigm for Parallel Programmable SoCs*, International IEEE Northeast Workshop on Circuits and Systems (IEEE-NEWCAS), 2006 (Invited Paper).

U. Aydonat and T. S. Abdelrahman, *Parallelization of Multimedia Applications on the Multi-Level Computing Architecture*, IASTED International Conference on Parallel and Distributed Computing and Systems (PDCS), pp. 438-447, 2006 (Received Best Paper Award in Applications).

F. Karim, A. Mellan, A. Nguyen, U. Aydonat, T. S. Abdelrahman, *A Multi-Level Computing Architecture For Multimedia Applications*, IEEE MICRO Journal, vol. 24, no. 3, pp. 55-66, May-June 2004. Also appears in ST Journal of Research, vol. 1, no. 2, pp. 4-16, 2004.

F. Karim, A. Mellan, U. Aydonat, T. S. Abdelrahman, *The Hyperprocessor: A Template System-on-Chip Architecture For Embedded Multimedia Applications*, Workshop on Application Specific Processors (WASP), pp. 66-73, 2003.

RELEVANT COURSEWORK

Computer Architecture, Software Engineering, Runtime Program Optimization, Modern and Emerging Architectures, Optimizing Compilers, Design and Implementation of Operating Systems, Compilation Techniques for Parallel Processors, Parallel Programming.

AWARDS

- ◇ Ewing Rae Graduate Scholarship at the University of Toronto in 2009.
- ◇ Best Paper Award in applications at the Conference on Parallel and Distributed Computing and Systems (PDCS) in 2006.
- ◇ University of Toronto Fellowship between 2005 and 2009.
- ◇ Completed the Bachelor of Science program with a GPA within the top 10% of 220 classmates.
- ◇ Ranked 200th among 1.5 million candidates in the Nationwide University Entrance Exam of Turkey in 1997.